

WHAT IS CLAIMED IS:

1 1. A receive path circuit in a radio frequency (RF)
2 receiver comprising:
3 a local oscillator (LO) circuit capable of receiving a
4 local oscillator (LO) reference signal having frequency, LO, and
5 a double sideband (DSB) clock signal having a frequency, DSB, and
6 generating therefrom an in-phase product signal of said LO
7 reference signal and said DSB clock signal in which a polarity of
8 said LO reference signal is reversed at said DSB frequency of
9 said DSB clock signal; and
10 a first radio frequency (RF) mixer having a first input
11 port capable of receiving said in-phase product signal from said
12 LO circuit and a second input port capable of receiving a
13 modulated radio frequency (RF) signal, wherein said first RF
14 mixer generates a first downconverted output signal.

1 2. The receive path circuit as set forth in Claim 1
2 wherein said LO circuit is further capable of generating a
3 quadrature phase product signal from said LO reference signal and
4 said DSB clock signal, wherein said quadrature phase signal is
5 shifted approximately 90 degrees with respect to said in-phase
6 product signal and wherein a polarity of said LO reference signal
7 is reversed at said DSB frequency of said DSB clock signal.

1 3. The receive path circuit as set forth in Claim 2
2 further comprising a second radio frequency (RF) mixer having a
3 first input port capable of receiving said quadrature phase
4 product signal from said LO circuit and a second input port
5 capable of receiving said modulated radio frequency (RF) signal,
6 wherein said second RF mixer generates a second downconverted
7 output signal.

1 4. The receive path circuit as set forth in Claim 3
2 wherein said LO circuit comprises a multiplier that receives an
3 in-phase LO reference signal and said DSB clock signal and
4 generates therefrom said in-phase product signal.

1 5. The receive path circuit as set forth in Claim 4
2 wherein said multiplier is an analog multiplier.

1 6. The receive path circuit as set forth in Claim 4
2 wherein said multiplier is an exclusive-OR gate.

1 7. The receive path circuit as set forth in Claim 3
2 wherein said first downconverted output signal of said first RF
3 mixer is a double-sideband suppressed carrier signal.

1 8. The receive path circuit as set forth in Claim 7
2 wherein said second downconverted output signal of said second RF
3 mixer is a double-sideband suppressed carrier signal.

1 9. The receive path circuit as set forth in Claim 8
2 further comprising a first DSB filter block capable of receiving
3 said first downconverted output signal from said first RF mixer
4 and said DSB clock signal, wherein said first DSB filter block
5 reverses a polarity of said first downconverted output signal at
6 said DSB frequency of said DSB clock signal to thereby produce an
7 in-phase baseband output signal.

1 10. The receive path circuit as set forth in Claim 9
2 further comprising a second DSB filter block capable of receiving
3 said second downconverted output signal from said second RF mixer
4 and said DSB clock signal, wherein said second DSB filter block
5 reverses a polarity of said second downconverted output signal at
6 said DSB frequency of said DSB clock signal to thereby produce a
7 quadrature phase baseband output signal.

1 11. A radio frequency (RF) receiver comprising:

2 a receiver front-end circuit capable of receiving an
3 incoming RF signal from an antenna and filtering and amplifying
4 said incoming RF signal;

5 a local oscillator (LO) circuit capable of receiving a
6 local oscillator (LO) reference signal having frequency, LO, and
7 a double sideband (DSB) clock signal having a frequency, DSB, and
8 generating therefrom an in-phase product signal of said LO
9 reference signal and said DSB clock signal in which a polarity of
10 said LO reference signal is reversed at said DSB frequency of
11 said DSB clock signal; and

12 a first radio frequency (RF) mixer having a first input
13 port capable of receiving said in-phase product signal from said
14 LO circuit and a second input port capable of receiving said
15 filtered and amplified incoming RF signal, wherein said first RF
16 mixer generates a first downconverted output signal.

1 12. The radio frequency (RF) receiver as set forth in
2 Claim 11 wherein said LO circuit is further capable of generating
3 a quadrature phase product signal from said LO reference signal
4 and said DSB clock signal, wherein said quadrature phase signal
5 is shifted approximately 90 degrees with respect to said in-phase
6 product signal and wherein a polarity of said LO reference signal
7 is reversed at said DSB frequency of said DSB clock signal.

1 13. The radio frequency (RF) receiver as set forth in
2 Claim 12 further comprising a second radio frequency (RF) mixer
3 having a first input port capable of receiving said quadrature
4 phase product signal from said LO circuit and a second input port
5 capable of receiving said filtered and amplified incoming RF
6 signal, wherein said second RF mixer generates a second
7 downconverted output signal.

1 14. The radio frequency (RF) receiver as set forth in
2 Claim 13 wherein said LO circuit comprises a multiplier that
3 receives an in-phase LO reference signal and said DSB clock
4 signal and generates therefrom said in-phase product signal.

1 15. The radio frequency (RF) receiver as set forth in
2 Claim 14 wherein said multiplier is an analog multiplier.

1 16. The radio frequency (RF) receiver as set forth in
2 Claim 14 wherein said multiplier is an exclusive-OR gate.

1 17. The radio frequency (RF) receiver as set forth in
2 Claim 13 wherein said first downconverted output signal of said
3 first RF mixer is a double-sideband suppressed carrier signal.

1 18. The radio frequency (RF) receiver as set forth in
2 Claim 17 wherein said second downconverted output signal of said
3 second RF mixer is a double-sideband suppressed carrier signal.

1 19. The radio frequency (RF) receiver as set forth in
2 Claim 18 further comprising a first DSB filter block capable of
3 receiving said first downconverted output signal from said first
4 RF mixer and said DSB clock signal, wherein said first DSB filter
5 block reverses a polarity of said first downconverted output
6 signal at said DSB frequency of said DSB clock signal to thereby
7 produce an in-phase baseband output signal.

1 20. The radio frequency (RF) receiver as set forth in
2 Claim 19 further comprising a second DSB filter block capable of
3 receiving said second downconverted output signal from said
4 second RF mixer and said DSB clock signal, wherein said second
5 DSB filter block reverses a polarity of said second downconverted
6 output signal at said DSB frequency of said DSB clock signal to
7 thereby produce a quadrature phase baseband output signal.